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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/945,084	08/30/2001	Rich Fogal	2001-0128.00	3141
7590	06/29/2004		EXAMINER	NGUYEN, KHIEM D
Kevin D. Martin Agent for Applicant Micron Technology, Inc. 8000 S. Federal Way, MS 525 Boise, ID 83716			ART UNIT	PAPER NUMBER
			2823	
DATE MAILED: 06/29/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/945,084	FOGAL ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 26 April 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 33-46 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 33-46 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 30 August 2001 is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.

 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s). ____ .
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application (PTO-152)
3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ . 6) Other: ____ .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 26th, 2004 has been entered. A new rejection is made as set forth in this Office Action. Claims (33-46) are pending in the application.

Claim Objections

Claims 33 35, and 37 are objected to because of the following informalities: The Examiner objects to the terms "if", "could", and "were" because these terms are not positive inventive process steps, and do not provide no further limitation to the invention and are not enforceable. Appropriate correction is required.

Claim 35 recites the limitation "the memory device" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 44 is objected to because of the following informalities: In claim 44, line 1, delete "420", and insert -- 42 --. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 33-35 are rejected under 35 U.S.C. 102(b) as being anticipated by (JP 6-232537).

In re claim 33, JP 6-232537 discloses a method of manufacturing a semiconductor device, comprising: forming a first circuit (**FIGS. 3a-c: 11**, located on the left side) and a second circuit (**FIGS. 3a-c: 11**, located on the right side) on a semiconductor wafer substrate assembly; forming a first conductor connected to the first semiconductor circuit and a second conductor connected to the second semiconductor circuit (JP 6-232537 English translation, page 1, paragraph [0005] and **FIGS. 3a-c**), wherein the first conductor is electrically separated from the second conductor such that the first and second circuits are sufficiently isolated to provide protection to the second circuit (**FIGS. 3a-c**); with the first and second circuits electrically separate from each other, performing an electrical operation on the first circuit with a voltage which could damage the second circuit if the first and second circuits were not electrically separate (English translation, pages 1-2); subsequent to performing the electrical operation on the first circuit, shorting the first and second conductors together to electrically couple the first and second circuits (**FIGS. 3b-c**); and subsequent to shorting the first and second conductors together (**FIGS. 3c: 14**), encapsulating the semiconductor wafer substrate assembly (JP 6-232537 English translation, pages 1-2 and **FIGS. 1-3**).

In re claim 34, JP 6-232537 discloses wherein the method of claim 33 further comprising shorting the first and second conductor together with a ball bond (**FIG. 3c: 14**) (English translation, page 1, paragraph [0005]).

In re claim 35, JP 6-232537 discloses wherein the first and second circuits are fabricated such that the memory device is inoperative if the first and second conductors remain electrically separate subsequent to encapsulation (English translation, pages 1-2 and **FIGS. 1-3**).

2. Claims 37-40 are rejected under 35 U.S.C. 102(b) as being anticipated by (JP 6-232537).

In re claim 37, JP 6-232537 discloses a method of manufacturing a memory device, comprising: forming a plurality of primary and redundant memory cell locations; forming antifuse circuitry which allows selection of the redundant memory cell locations; forming voltage sensitive circuitry on the semiconductor wafer substrate assembly; forming a first conductor (**FIGS. 3a-c: 11** located on the left side) electrically connected with the antifuse circuitry; forming a second conductor (**FIGS. 3a-c: 11** located on the right side) electrically connected with the voltage sensitive circuitry, wherein the first and second conductors are electrically separated from each other (**FIG. 3a**); while the first and second conductors are electrically separated, applying a sufficient voltage to the antifuse circuitry to program the antifuse circuitry, wherein the sufficient voltage could damage the voltage sensitive circuitry if the first and second conductors were electrically connected (English translation, pages 1-2); and subsequent to programming the antifuse circuitry, electrically shorting the first conductor with the second conductor (**FIG. 3c: 14**) (English translation, page 1, paragraph [0005]).

In re claim 38, JP 6-232537 discloses wherein the method of claim 37 further comprising encapsulating the antifuse circuitry, the voltage sensitive circuitry, the first

conductor, and the second conductor subsequent to electrically shorting the first conductor with the second conductor (English translation, page 2).

In re claim 39, JP 6-232536 discloses wherein the method of claim 37 further comprising electrically shorting the first conductor with the second conductor using a ball bond (**FIG. 3c: 14**) (English translation, page 1, paragraph [0005]).

In re claim 40, JP 6-232536 discloses wherein the antifuse circuitry and the voltage sensitive circuitry are fabricated such that the memory device is inoperative if the first and second conductors remain electrically separated (English translation, pages 1-2 and **FIGS. 1-3**).

3. Claims 42-45 are rejected under 35 U.S.C. 102(b) as being anticipated by (JP 6-232537).

In re claim 42, JP 6-232537 discloses a method of manufacturing a memory device comprising: fabricating first and second circuits on a semiconductor wafer substrate assembly, wherein the first and second circuits are adapted to be electrically connected through a common conductor 11 (**FIGS. 3a-c**); fabricating the common conductor with a physical opening to provide an open circuit (predetermined gap) between the first and second circuits (English translation, page 1, paragraph [0005] and **FIG. 3a**), such that the first circuit is sufficiently isolated from the second circuit to provide protection for the first circuit from a voltage applied to the second circuit (English translation, page 1, paragraph [0005]); applying the voltage to the second circuit; and subsequent to applying the voltage to the second circuit, bridging the physical opening of the common conductor to electrically connect the first and second circuits together (**FIG. 3c: 14**) (English translation, page 1, paragraph [0005]).

In re claim 43, JP 6-232537 discloses wherein the method of claim 42 further comprising encapsulating the first and second circuits and the common conductor subsequent to bridging the physical opening (English translation, page 2).

In re claim 44, JP 6-232536 discloses wherein the method of claim 42 further comprising bridging the physical opening with a ball bond (**FIG. 3c: 14**) (English translation, page 1, paragraph [0005]).

In re claim 45, JP 6-232536 discloses wherein the first and second circuits are fabricated such that the memory device is inoperative if the physical opening remains unbridged (English translation, pages 1-2 and **FIGS. 1-3**).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 36, 41, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over (JP 6-232537) in view of the applicant's admitted prior art (AAPA) of this application.

In re claims 36, 41, and 46, AAPA discloses providing a lead frame, and subsequent to shorting the first and second conductors together, attaching the semiconductor wafer substrate assembly to the lead frame (page 4, paragraph [0010]). It would have been obvious to one of ordinary skill in the art of making semiconductor

devices to combine the teaching of JP 6-232537 and AAPA in such a way that the lead frame and die are encapsulated or otherwise packaged (page 4, paragraph [0010]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
June 25, 2004



W. DAVID COLEMAN
PRIMARY EXAMINER